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2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,713	PETTEY ET AL.	
	Examiner	Art Unit	
	Trisha Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01-14-04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21,06/07,09/01,09/22,01/11,08/01,05/13*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-76 are presented for examination.

Specification and Claim Objections

2. Claim 24 is objected to because of the following informalities: "***Deterining***" (line 3) should be changed to "***determining***". Appropriate correction is required.

3. Claim 31 recites the limitation "each of ***the plurality of root complexes***" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

4. Claim 54 recites the limitation "***said table lookup***" in line 3. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter: "PCI Express Architecture is a base specification 1.0 that ***does not include provisions for sharing I/O***" (claim 3). See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> ***The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.***

6. Claims 35, 55, 68 and 76 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter "***PCI Express+***" which was not described in the specification in such a way as to enable one skilled in the art to

which it pertains, or with which it is most nearly connected, to make and/or use the invention.

For purpose of Examination, "PCI Express+" has been interpreted as "PCI Express".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 3 and 36-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

a. Regarding claim 3: "said PCI Express Architecture is a base specification 1.0 that ***does not include provisions for sharing I/O***" is not clear. First, it is not clear what "***provisions for sharing I/O***" is, since there is no support for this in the Specification. Second, it is not clear whether or not PCI Express Architecture Base Specification 1.0 originally includes "***provisions for sharing I/O***".

Case 1: If PCI Express Architecture Base Specification 1.0 originally does not include "***provisions for sharing I/O***", then it is obvious true that "PCI Express Architecture Base Specification 1.0 ***does not include provisions for sharing I/O***", since it is just an inherent feature in PCI Express Architecture Base Specification 1.0.

Case 2: If PCI Express Architecture Base Specification 1.0 originally includes "***provisions for sharing I/O***" and Applicant is claiming "said PCI Express Architecture is a base specification 1.0 that ***does not include provisions for sharing I/O***", then it is not clear why Applicant is using this PCI Express Specification and excluding its "***provisions for sharing I/O***" feature.

b. Regarding claims 36-39: note "***said second link comprises said first link*** plus an embedded field for storing said header" (lines 2-3 of claim 36). First, it is confusing that ***the second link comprises the first link*** since they are being claimed earlier in claim 27 as two different links: ***a first link*** between each of the plurality of OSDs and a shared I/O switch, ***a second link*** between said shared I/O switch and each of the plurality of endpoints. Second, it is not clear how ***the second link*** can ***comprise*** the first link plus ***an embedded field for storing said header*** since as claimed earlier in claim 27 "said ***shared I/O switch*** associating packets... by ***embedding a header*** within the packet", thus ***the second link cannot comprise an embedded field for storing said header***. It is possible saying that the switch or the packet comprises an embedded field for storing said header, but it does not make sense saying the link comprises an embedded field for storing said header, because the link is just a communicating connection to deliver data; unless Applicant defines the link differently.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 9-11, 13-19, 23, 25-26, 44, 48-49, 52-54, 56-57, 60, 69-73 and 75 are rejected under 35 U.S.C. 102(b)/(e) as being anticipated by Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya).

Regarding claim 1, Athreya teaches a shared input/output (I/O) fabric within a load/store domain (note Figures. 2A, 3A, 5, and similarly in other Figures), comprising: a plurality of root complexes (e.g. Networks 52, 54, 56 and associated circuitry - Fig. 2A, or networks 74, 76, 78 and associated circuitry - Fig. 3A, or similarly in other Figures); a shared I/O switch (Tagging Unit 86, or Tagging Unit 86 and associated circuitry such as Switch 88) coupled to said plurality of root complexes; and a shared I/O controller (e.g. Switch 88 or Router 90 in Fig. 3, or Switch 132 in Fig. 5), coupled to said shared I/O switch; wherein said shared I/O switch receives packets from each of said plurality of root complexes, places root complex identification (VLAN ID) within said packets for use by said shared I/O controller, and transmits said packets with said root complex identification to said shared I/O controller for processing (Fig. 3B and paragraph [0040]).

Regarding claim 9, Athreya further teaches none of said plurality of root complexes includes a dedicated network interface controller (e.g. Figs. 2A, 3A)

Regarding claim 10, Athreya further teaches each of said plurality of root complexes comprise at least one port (logical interface port) for coupling to said shared I/O switch (networks 74, 76 and 78 are associated with different input WAN logical port interfaces for the unit 86, Fig. 3A and paragraph [0040]).

Regarding claim 11, Athreya further teaches said port conforms to a serial load/store architecture (e.g. interface port which receives 802.3 frame, Figs. 2A and 2B).

Regarding claim 13, Athreya further teaches said shared I/O switch comprises a plurality of ports (e.g. unit 86 comprises a plurality of interface ports associated with different networks 74, 76, and 78, paragraph [0040]).

Regarding claim 14, Athreya further teaches each of said plurality of root complexes is coupled to at least one of said plurality of ports to allow communication there between (e.g. unit 86 comprises a plurality of interface ports associated with different networks 74, 76, and 78, paragraph [0040]).

Regarding claim 15, Athreya further teaches said shared I/O switch receives a packet (e.g. 802.3 frame in Fig. 2B or unbridged striped frame in Fig. 3B) from one of said plurality of root complexes, it identifies which of said one of said plurality of root complexes transmitted said packet based on a port within said shared I/O switch coupled to said one of said plurality of root complexes (identifying based on the port from which the packet is transmitted, Figs. 2B, 3B, and paragraphs [0038-0040]).

Regarding claim 16, Athreya further teaches the port is associated with a bus hierarchy within the load/store domain (note the links at the port interface in Figs. 2A, 3A).

Regarding claim 17, Athreya further teaches said shared I/O switch places said root complex identification (VLAN ID) in said packet based upon said port (Fig. 3B and paragraph [0040]).

Regarding claim 18, Athreya further teaches said shared I/O switch associates said one of said plurality of root complexes that transmitted said packet with said one of

said plurality of root complexes based on a PCI bus hierarchy (based on the port interface connected to PCI bus 158) within said shared I/O switch (Fig. 10).

Regarding claim 19, Athreya further teaches the association by said shared I/O switch utilizes a lookup table (VLAN table, paragraphs [0039-0040]).

Regarding claim 23, Athreya further teaches said shared I/O controller further comprises a bus interface for determining which of said plurality of root complexes is identified within said packets (e.g. Figs. 2A, 2B and paragraphs [0038-0040]).

Regarding claim 25, Athreya further teaches wherein a bus interface within said shared I/O controller places said root complex identification (VLAN ID) within packets destined for said plurality of root complexes to allow said shared I/O switch to transmit said packets to an appropriate one of said plurality of root complexes (e.g. Figs. 2A, 2B and paragraphs [0038-0040]).

Regarding claim 26, Athreya further teaches said root complex identification comprises a plurality of bits which are inserted within said packets between said shared I/O switch and said shared I/O controller (e.g. note Fig. 3B wherein VLAN ID = 20).

Regarding claim 44, Athreya teaches an apparatus for associating packets in a load/store serial communication fabric (e.g. note Figures. 2A, 3A, 5, and similarly in other Figures) with root complexes (e.g. networks 74, 76, 78 in Fig. 3) to allow the root complexes to share an input/output (I/O) endpoint (e.g. Switch 88 or Router 90 in Fig. 3, or Switch 132 in Fig. 5), the apparatus comprising: a shared I/O switch, coupled to each of the root complexes, said shared I/O switch (Tagging Unit 86, or Tagging Unit 86 and associated circuitry such as Switch 88) having routing control (VLAN table and

associated circuitry) to associate the packets from each of the root complexes with the root complex they originate from by incorporating a field within the packets (VLAN ID, paragraph [0040]); and a link between said shared I/O switch and the input/output (I/O) endpoint (note the link in Figs 2A, 3A), wherein said link allows the packets to be transferred from said shared I/O switch to the input/output (I/O) endpoint with said field; wherein the input/output (I/O) endpoint associates the packets with their associated root complexes by examining said field (paragraph [e.g. Fig. 3B and paragraph [0040], or Figs. 5-7 and paragraph [0045]).

Regarding claim 48, Athreya further teaches the root complexes comprises processing complexes (networks 74, 76, 78 - Fig. 3, are processing complexes since they at least can process data received and data to be sent out).

Regarding claim 49, Athreya further teaches the input/output (I/O) endpoint comprises a shared network interface controller (e.g. shared switch 132 in Fig. 5 wherein switch 132 can send data to different networks 134 or 136 depending upon the VLAN ID).

Regarding claim 52, Athreya further teaches said shared I/O switch comprises: a plurality of ports (interface ports at the switch, note Fig. 2A, 3A, or 5) for connecting said shared I/O switch to the root complexes and to the input/output (I/O) endpoint, wherein at least one of the plurality of ports is associated with each of the root complexes, and at least one of the plurality of ports is associated with the input/output (I/O) endpoint; and said routing control, coupled to said plurality of ports, wherein said routing control is

aware of which of said plurality of ports is associated with which of the root complexes (paragraph [0040]).

Regarding claim 53, Athreya further teaches said routing control comprises a table lookup (VLAN table) that associates each of the plurality of ports with the root complexes (e.g. Fig. 2B and paragraph [0039]).

Regarding claim 54, Athreya further teaches said field includes information from a table lookup (VLAN table) to associate the packets with their root complexes (e.g. Fig. 2B and paragraph [0039]).

Regarding claim 56, Athreya further teaches the input/output (I/O) endpoint contains packets from more than one of the root complexes at the same time ([paragraph [0041-0043]).

Regarding claim 57, Athreya teaches a method for associating packets, within a serial load/store fabric (note Figures. 2A, 3A, 5, and similarly in other Figures), from a plurality of root complexes (e.g. networks 74, 76, 78 in Fig. 3) with their originating root complex, to allow the plurality of root complexes to share an I/O endpoint (e.g. Switch 88 or Router 90 in Fig. 3, or Switch 132 in Fig. 5), the method comprising: providing a first link between the plurality of root complexes and a switch (Tagging Unit 86, or Tagging Unit 86 and associated circuitry such as Switch 88), the packets in the first link unaware that the root complexes are sharing the I/O endpoint; within the switch, embedding a header in the packets to associate the packets with their originating root complex (VLAN ID); providing a second link between the switch and the I/O endpoint, the second link capable of communicating the packets with the embedded header between the switch and

the I/O endpoint; and at the I/O endpoint, examining the packets with the embedded header to allow the I/O endpoint to associate each of the packets with their originating root complex (e.g. Fig. 3B and paragraph [0040], or Figs. 5-7 and paragraph [0045], also note the links as shown in the Figures).

Regarding claim 60, Athreya further teaches a first one of the root complexes comprises a processing complex (networks 74, 76, 78 in Fig. 3).

Regarding claim 69, Athreya further teaches said step of embedding comprises: determining which port within the switch a packet is received from; associating the packet with that port; and assigning a header number (VLAN ID) to the packet associating the packet with a bus hierarchy for the port which received the packet (e.g. paragraph [0040])).

Regarding claim 70, Athreya further teaches said step of associating the packet comprises: performing a table lookup from a table (VLAN Table) which correlates that port with its associated root complex (e.g. Fig. 2B and paragraph [0039]).

Regarding claim 71, Athreya further teaches a plurality of packets with embedded headers from a plurality of root complexes reside in the I/O endpoint at the same time ([paragraph [0041-0043]).

Regarding claim 72, Athreya teaches a method for partitioning I/O devices (e.g. networks 134, 136) among a plurality of processing complexes (e.g. networks 112, 114, 116, Fig. 5), the partitioning performed within the load/store domain of each of the processing complexes, the method comprising: providing a switch (e.g. VLAN Unit 130 and associated circuitry) between the I/O devices and the plurality of processing

complexes, the switch utilizing a first load/store fabric between the plurality of processing complexes and the switch (note links between networks 112, 114, 116 and the switch, and a second load/store fabric between the switch and the I/O devices (note links between the switch and networks 134, 136); mapping each of the plurality of processing complexes to one or more of the I/O devices; and transferring packets between the plurality of processing complexes to the I/O devices based upon said mapping (paragraph [0045]); wherein at least one of the I/O devices is mapped to only one of the plurality of processing complexes (e.g. note VLAN table in Fig. 6 wherein the network device 134 (ID=20) is mapped to only one network 114 (logical interface B)); and wherein at least one of the I/O devices is mapped to two or more of the plurality of processing complexes (e.g. note VLAN table in Fig. 6 wherein network device 136 (ID=10) is mapped to two networks 112 and 116 (logical interfaces A and C).

Regarding claim 73, Athreya further teaches the switch is a shared I/O switch (switch VLAN unit 130 is shared by plurality of networks, Fig. 5).

Regarding claim 75, Athreya further teaches the switch of said step of providing utilizes a second load/store fabric between the switch and the I/O devices that includes header information associating packets with their processing complexes (paragraph [0045]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-3, 12, 45-46, 51, 55, 61, 67-68, 74 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya) in view of Boom et al. (U.S. Pub. No. 2004/0073716) (hereinafter Boom).

Regarding claim 2, the argument above for claim 1 applies. However, Athreya does not explicitly disclose the shared input/output (I/O) fabric utilizes a PCI Express Architecture. Boom teaches PCI Express Architecture (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement PCI Express Architecture as taught by Boom in the system of Athreya because PCI Express is a well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

Regarding claim 3, Boom further teaches said PCI Express Architecture is a base specification 1.0 that does not include provisions for sharing I/O (e.g. Fig. 4 and paragraph [0041]).

Regarding claim 12, the argument above for claim 10 applies. However, Athreya does not explicitly disclose the port conforms to PCI Express architecture. Boom teaches PCI Express Architecture (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to implement PCI Express Architecture as taught by Boom in the system of Athreya because PCI Express is a well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

Regarding claim 45, the argument above for claim 44 applies. However, Athreya does not explicitly disclose the packets are PCI Express packets. Boom teaches PCI Express Architecture (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement PCI Express Architecture as taught by Boom in the system of Athreya because PCI Express is a well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

Regarding claim 46, the argument above for claim 44 applies. However, Athreya does not explicitly disclose the root complexes (e.g. networks 74, 76, 78 in Fig. 3) comprise: a component in a PCI Express hierarchy that connects to a host bus segment on an upstream side with one or more PCI Express links on a downstream side. Boom teaches root complex comprising: a component in a PCI Express hierarchy that connects to a host bus segment (e.g. note the link connection to CPU 312) on an upstream side with one or more PCI Express links (e.g. note the link connection to Switch 316) on a downstream side (Fig. 4 and paragraph [0041]). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to implement each root complex in Athreya's system to comprise a component in a PCI Express hierarchy that connects to a host bus segment on an upstream side with one or more PCI Express links on a downstream side as taught by Boom to provide a host processing system (paragraph [0041]), also PCI Express link is a well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

Regarding claim 51, the argument above for claim 44 applies. However, Athreya does not explicitly disclose the load/store serial communication fabric utilizes PCI Express. Boom teaches PCI Express serial communication (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement PCI Express serial communication as taught by Boom in the system of Athreya because PCI Express is a well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

Regarding claim 55, the argument above for claim 44 applies. However, Athreya does not explicitly disclose the link comprise PCI Express link. Boom teaches PCI Express communication (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement PCI Express communication as taught by Boom in the system of Athreya because PCI Express is a

well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

Regarding claim 61, the argument above for claim 60 applies. However, Athreya does not explicitly disclose the processing complex comprises: one or more processors; and memory, coupled to said one or more processors for storing data utilized by said one or more processors. Boom teaches processing complex (Root complex 318 and associated circuitry such as CPU 312 and Memory 314) comprising: one or more processors (CPU 312); and memory (System Memory 314), coupled to said one or more processors for storing data utilized by said one or more processors (Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the processing complex of Athreya to comprise one or more processors; and memory, coupled to said one or more processors for storing data utilized by said one or more processors as taught by Boom to provide the system the function of a host processing system (paragraph [0041]).

Regarding claims 67 and 68, the argument above for claim 57 applies. However, Athreya does not explicitly disclose the first link and the second link comprise PCI Express links. Boom teaches PCI Express communication (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement PCI Express communication as taught by Boom in the system of Athreya because PCI Express is a well-known and widely used standard in the art which

provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

Regarding claims 74 and 76, the argument above for claim 72 and 75 apply. However, Athreya does not explicitly disclose the first load/store fabric and the second load/store fabric comprise PCI Express. Boom teaches PCI Express Architecture (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement PCI Express Architecture as taught by Boom in the system of Athreya because PCI Express is a well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

10. Claims 4-8, 20-22, 24 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya) in view of Lee et al. (U.S. Patent 6,823,458) (hereinafter Lee).

Regarding claim 4, the argument above for claim 1 applies. However, Athreya does not explicitly disclose the plurality of root complexes comprise a plurality of operating system domains (OSD's). Lee teaches multiple operating system domains (Figs. 1-2, col. 2 lines 53-65 and col. 3 lines 35-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the root complexes comprising a plurality of operating system domains as taught by Lee in the

system of Athreya to provide the system with multiple concurrently running operating systems as desired by user (col. 2 lines 53-60).

Regarding claim 5, Lee further teaches each of said plurality of OSD's has an operating system (col. 3 lines 35-42).

Regarding claim 6, Lee further teaches at least one of said plurality of OSD's executes an operating system that is different from other ones of said plurality of OSD's (e.g. Windows, Linux, etc., col. 3 lines 35-42).

Regarding claim 7, the argument above for claim 4 applies. However, Athreya does not explicitly disclose each of said plurality of OSD's comprise: a processing complex; and memory, coupled to said processing complex for storing data to be utilized by said processing complex. Lee further teaches each OSD (210, 220, 230) comprises a processing complex and memory, coupled to said processing complex for storing data to be utilized by said processing complex (note col. 3 lines 34-42 wherein devices 210, 220, 230 may be any type of processing devices including personal computers, mainframe computers, PDA, etc..., thus it is inherent that there must be a memory for storing data to be utilized by the processing complex in the computer). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the OSD comprising a processing complex and memory, coupled to said processing complex for storing data to be utilized by said processing complex as taught by Lee in the system of Athreya so that the communicating system includes additional functions and devices (computers, PDAs, etc.) as desired by user.

Regarding claim 8, Lee further teaches said processing complex comprises one or more processors (this is inherent since the computer or PDA must have at least a processing device).

Regarding claim 20, the argument above for claim 1 applies. However, Athreya does not explicitly disclose said shared I/O controller comprises: a plurality of OS Domain portions. Lee teaches shared I/O controller (server 240 and associated circuitry) comprising a plurality of OS Domain portions (Figs. 1-2, col. 2 lines 53-65 and col. 3 lines 35-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the shared I/O controller comprising a plurality of OS Domain portions as taught by Lee in the system of Athreya to provide the system with multiple concurrently running operating systems as desired by user (col. 2 lines 53-60).

Regarding claim 21, Lee further teaches each of said plurality of OS Domain portions comprise control registers (virtual devices 250-270, note that virtual devices are created using software or hardware and may consist of virtual disk files, capable of running a plurality of operating systems, col. 3 lines 58-65, therefore the OS portions comprise control registers).

Regarding claim 22, Lee further teaches each of said plurality of OS Domain portions further comprise a descriptor (identifier assigned and stored by controller 240 which uniquely identifies the client 210-230, the OS being used, etc., col. 4 line 66 to col. 5 line 11).

Regarding claim 24, Lee further teaches said shared I/O controller further comprises a bus interface for determining which of a plurality of operating system

domains (OSD's) is identified within said packets (controller 240 checks the identifier included in the received packet and determines the OSD, col. 4 line 37 to col. 5 line 11).

Regarding claim 47, the argument above for claim 44 applies. However, Athreya does not explicitly disclose the root complexes comprise operating system domains (OSD's). Lee teaches multiple operating system domains (Figs. 1-2, col. 2 lines 53-65 and col. 3 lines 35-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the root complexes comprising a plurality of operating system domains as taught by Lee in the system of Athreya to provide the system with multiple concurrently running operating systems as desired by user (col. 2 lines 53-60).

11. Claims 27, 28, 31, 33, 34, 36-43, 58, 59 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya) in view of Dove et al. (U.S. Pub. No. 2004/0202013) (hereinafter Dove).

Regarding claim 27, Athreya teaches a serial communication architecture (note Figures. 2A, 3A, 5, and similarly in other Figures) between a plurality of networks (e.g. Networks 52, 54, 56 and associated circuitry - Fig. 2A, or networks 74, 76, 78 and associated circuitry - Fig. 3A, or networks 112, 114, 116 – Fig. 5, or similarly in other Figures) and a plurality of endpoints (e.g. connections at switch 132 to other networks 134, 136 – Fig. 5) to allow each of the plurality of networks to share each of the plurality of endpoints, the architecture comprising: a first link (note links connecting to Unit 130 at logical port interfaces A, B, C – Fig. 5), between each of the plurality of networks and a

shared I/O switch (Unit 130 and associated circuitry such as Switch 132 – Fig. 5); a second link (links to other networks 134, 136 – Fig. 5), between said shared I/O switch and each of the plurality of endpoints, said shared I/O switch associating packets from the plurality of networks with the networks by embedding a header (VLAN ID) within said packets before transmitting said packets to the plurality of endpoints (paragraphs [0045-0048]). However, Athreya does not explicitly disclose the networks comprise a plurality of operating system domains. Dove teaches networks (servers 300) comprising a plurality of operating system domains (Windows, Linux, etc...) (Fig. 1 and paragraph [0024]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the networks each have a different operating system domain as taught by Dove in the networks of Athreya because it provides an advantage of dynamic multi-mode system as desired by user (paragraph [0024]).

Regarding claim 28, Athreya further teaches the plurality of endpoints comprise: a first endpoint for network communication (e.g. to network 134 – Fig. 5). However, Athreya does not explicitly disclose the second endpoint for communication with data storage devices. Dove further teaches data storage devices (Data Storage 306 – Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include data storage devices as taught by Dove in one of the endpoints of Athreya so that the data storage devices can be shared among the multiple networks.

Regarding claim 31, Athreya further teaches each of the OSD (networks 112, 114, 116) communicates with a network (network 134) through said first endpoint (Fig. 5).

Regarding claim 33, Athreya further teaches said first link is replicated for each of the plurality of OSD's and said shared I/O switch (Fig. 5).

Regarding claim 34, Athreya further teaches said shared I/O switch comprises a plurality of ports (port interfaces A, B, C, D), at least one of said ports associated with each one of the plurality of OSD's (Fig. 5).

Regarding claim 36, Athreya further teaches an embedded field for storing said header (VLAN ID) (Figs. 6-7 and paragraphs [0045-0048]).

Regarding claim 37, Athreya further teaches said embedded field associates a packet from one of the plurality of OSD's with that one of the plurality of OSD's (paragraph [0047]).

Regarding claim 38, Athreya further teaches said embedded field comprises bit field for associating said packets with a number of OSD's (paragraphs [0036], [0045] and Fig. 3B). Even though, Athreya and Dove do not explicitly specify the number of OSDs in the system and the number of bits in the embedded field, however, since the system can work with any number of OSDs, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement 64 distinct one of OSDs as desired by user. Also, implementing the ID field comprising 6 bits for associating the packets with the OSDs is within the knowledge of ordinary skill in the art. One of ordinary skill in the art would motivate to implement 6-bit field for associating 64 distinct OSDs because 6-bit field yields 64 distinct IDs (6-bit $\rightarrow 2^6 = 64$ combinations).

Regarding claim 39, Athreya further teaches said embedded field associates said packets with ones of the plurality of OSD's utilizing a plurality of bit fields (Figs. 3B, 6-7).

Regarding claim 40, Athreya further teaches said header is transmitted with said packets from said shared I/O switch to at least one of the plurality of endpoints (paragraphs [0045-0048]).

Regarding claim 41, Athreya further teaches said at least one of the plurality of endpoints utilizes said header to determine which of the plurality of OSD's it is performing processing for (this is inherent in the system of Athreya and Dove, since each network is associated with a distinct OSD, and the header provides information of the requesting network).

Regarding claim 42, Athreya further teaches each of the plurality of endpoints performs processing for at least two of the plurality of OSD's (e.g. Network 136 with VLAN ID=10 is associated with two Networks 112 and 116, Figs. 5-6).

Regarding claim 43, Athreya further teaches said packets from at least two of the plurality of OSD's reside within said at least one of the plurality of endpoints at the same time (e.g. Network 136 with VLAN ID=10 is associated with two Networks 112 and 116, Figs. 5-6).

Regarding claims 58, 59 and 62, the argument above for claim 57 applies. However, Athreya does not explicitly disclose the root complexes are network computer servers having different operating systems. Dove teaches network computer servers (servers 300) having different operating systems (Windows, Linux, etc...) (Fig. 1 and

paragraph [0024]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement network computer servers having different operating systems as taught by Dove in the root complexes of Athreya because running independent operating systems for servers provides an advantage of dynamic multi-mode system as desired by user (paragraph [0024]).

12. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya) in view of Dove et al. (U.S. Pub. No. 2004/0202013) (hereinafter Dove) and further in view of Avery (U.S. Pub. No. 2003/0065822).

Regarding claims 29 and 30, the argument above for claim 27 applies. However, Athreya and Dove do not explicitly disclose the plurality of endpoints comprise a keyboard controller and a mouse controller, and further comprise a video controller. Avery teaches keyboard controller (125), mouse controller (135), and video controller (115) to be shared among a plurality of network servers (Figs. 1-2 and paragraphs [0019-0021]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include keyboard controller (125), mouse controller (135), and video controller (115) as taught by Avery in the system of Athreya and Dove so that keyboard, mouse, and video devices can be shared among the plurality of networks, eliminating a need for a console in every computer (paragraph [0021]).

13. Claims 32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya) in view of Dove et al. (U.S. Pub. No.

2004/0202013) (hereinafter Dove) and further in view of Boom et al. (U.S. Pub. No. 2004/0073716) (hereinafter Boom).

Regarding claims 32 and 35, the argument above for claim 27 applies. However, Athreya and Dove do not explicitly disclose the first link and the second link comprise PCI Express. Boom teaches PCI Express Architecture (PCI Express I/O architecture according to PCI Express Base Specification) (e.g. Fig. 4 and paragraph [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement PCI Express Architecture as taught by Boom in the system of Athreya because PCI Express is a well-known and widely used standard in the art which provides low cost, high performance, general purpose I/O interconnect defined for a wide variety of computing and communication platforms.

14. Claims 63-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya) in view of Silverman (U.S. Patent 6,731,649).

Regarding claims 63 and 64, the argument above for claim 57 applies. However, Athreya does not explicitly disclose the I/O endpoints comprises 1Gig Ethernet controller and 10 Gig Ethernet controller. Silverman teaches Ethernet controller (e.g. Ethernet Controller 208, Fig. 2) with 1 Gig or 10 Gig capacities (col. 7 lines 40-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement 1Gig or 10 Gig Ethernet controller as taught by Silverman in the system of

Athreya to provide a desired fast communication as Ethernet is a well-known standard in the art.

15. Claims 50, 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athreya et al. (US Pub. No. 2002/0027906) (hereinafter Athreya) in view of Wang et al. (U.S. Patent 6,834,326) (hereinafter Wang).

Regarding claim 50, the argument above for claim 44 applies. However, Athreya does not explicitly disclose the input/output (I/O) endpoint comprises a shared network storage controller. Wang teaches shared network storage controller (abstract and Figs. 5, 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the input/output (I/O) endpoint comprising a shared network storage controller as taught by Wang in the system of Athreya to allow the system to share storage devices.

Regarding claims 65 and 66, the argument above for claim 57 applies. However, Athreya does not explicitly disclose the I/O endpoint comprises a Fiber Channel controller or a serial ATA controller. Wang teaches shared network storage controller which can be implemented with different protocols including Fiber Channel, ATA, etc... as a matter of designer's choice (abstract and Figs. 5, 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the input/output (I/O) endpoint comprising storage controller as taught by Wang in the system of Athreya to allow the system to share storage devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Trisha Vu
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PAUL R. MYERS
PRIMARY EXAMINER